Avnet Design Services

Design of a Reconfigurable Video Peripheral

Introduction

Standards move so fast in the consumer video industry that a peripheral designed for a specific set of standards may become obsolete very quickly- maybe even faster than the design cycle for a new product. One solution to this type of problem is to create a hardware platform with enough flexibility to withstand even major changes in standards or feature set requirements using high capacity programmable logic like Field Programmable Gate Arrays, that can be updated even after the product is shipped to customers. Different standards could be selected by the customer and configured at the time of installation. Additional features can be offered to extend the lifetime of the product and can also be an additional revenue stream. This paper will describe the design of a flexible video peripheral that addresses these key customer requirements. The design of the system architecture, hardware platform and tool selection will all be described and can be used by designers when attacking any application with similar customer requirements, not just video applications.

Application Description

Field Programmable Gate Arrays, FPGAs, have grown sufficiently in capacity and functionality to support complete platforms on a single chip. It is now possible to implement processors, memories and high speed I/Os on a single FPGA. In addition to the high capacity and additional functionality, reprogrammable FPGAs also allow designs to be easily changed even after hardware has been designed. This capability allows versatile hardware to be designed as a platform on which applications can be developed, making it easier to hit moving standards or changing customer requirements. The consumer market has traditionally been a fast moving one with product cycle times of less than a year. Video and audio applications in particular have been a challenge. FPGA technologies are an especially attractive solution for these applications.

Manufacturers of embedded systems are also constantly striving to improve their customers' experiences with their products while increasing profit and market-share. These requirements can be satisfied through the use of the Xilinx Internet Reconfigurable Logic (IRL) design methodology. By updating the Xilinx PLD-based hardware design using the product's network connection instead of deploying field service technicians to the customer's site, maintenance costs can be reduced, increasing overall profitability. Furthermore, by extending the product's field life through instant updating of its features via a network connection, customer satisfaction – and market share – will increase. The PAVE framework from Xilinx can be used as a mechanism to remotely upgrade an application like a reconfigurable video peripheral. This application note will describe the approach to such a design in detail.

Architecture Description

The approach taken in this design is to create a flexible hardware design using only an FPGA and the necessary physical layer devices required by the target application market. The FPGA will provide all the functionality required by the application and will allow changes to be made even after the device is purchased by simply hooking the device to the Internet and downloading the code required by the specific device. Note that this also means that a single hardware platform can be used for multiple styles of a product (different feature sets) or even different application classes like peripherals or hosts. The use of a single hardware platform will simplify the manufacturing and support costs considerably.

The target application for the video processing peripheral is to interface between a variety of video devices and formats and allow a computer to capture, store, and operate on the video data stream. A block diagram of the system architecture is shown in figure 1. The video peripheral will accept video input from one of four sources -- the

Ethernet port, the USB port, the PCI bus or the PC Card interface. The video can be captured for processing by the computer or simply transferred from input port to output port as required by the user.

Because of the flexible nature of the hardware platform used in the design, new features can be offered to customers and reconfigured on demand. New bit files can be transferred via the Ethernet port, USB port, PCI bus or via the PC Card interface. The new bit file can then be stored into the on board flash memory so that the next time the FPGA is configured the new features are enabled. The Xilinx PAVE framework will be used to upgrade features in the field.

Use of the Xilinx PAVE Framework to Remotely Update Applications

Xilinx's PAVE interface is an API for the programming of Xilinx FPGAs in Wind River's VxWorks RTOS-based embedded systems. Previously, developers of field-upgradable applications had to develop their own software for interfacing the PLD programming methodology (JTAG or SelectMAP™) with Wind River's VxWorks RTOS. The PAVE interface encapsulates that design work into a set of commands covering configuration, readback, and utilities for verification. PAVE also includes a hardware design guideline for providing reliable fault-tolerant field upgrades in a uniform manner. For instance, PAVE can be used to create a rollback application that allows the system to return to the previous design, in case of network or power dropout during the upgrade process.

A system-level solution for creating field-upgradable hardware can be realized by using the PAVE interface. By combining this technology with Wind River's broad processor architecture support, a Xilinx FPGA can be configured from a remote server through the designer's C++ application and PAVE function calls in the target system. Designers wishing to use the PAVE framework for an application like the video processing peripheral can purchase the IRL Reference design from Avnet Design Services. (The Xilinx PMC IRL Reference Design Kit can be ordered from Avnet Design Services as ordering Part Number ADS-XLX-PMC-IRL and is priced at $2,495. For more information visit www.ads.avnet.com and click on Avnet Ave.)

IP Core Selection and Integration of the Video Processing Peripheral

In order to speed time to market and demonstrate the viability of the target application the design strategy was to use an off the shelf development board from Avnet Design Services, pre-developed Intellectual Property (IP) Cores from Xilinx, and a high productivity FPGA design tool from Celoxica.

Each of the peripheral signal sources (USB, PCI, Ethernet, and Card Bus) has a corresponding IP Core that is used to connect the physical layer interface to the internal data bus in the FPGA. These IP Cores are available from Xilinx and Xilinx Alliance Core partners and significantly speed the development process. The control of the capture and communication process is done within the FPGA using a Xilinx "MicroBlaze" soft processor core. This processor, available as an IP Core from Xilinx, provides the control of the flow of data from the various input, output and memory devices. Code for the processor is written in C and the GNU C compiler is used to create code for MicroBlaze. This portion of the design is not speed critical- it is control oriented- so a serial approach to execution was selected. (Avnet Design Services has a variety of MicroBlaze enabled development kits to accelerate the time to market for FPGA designs with embedded processing requirements. For more information visit www.ads.avnet.com and click on Avnet Ave.)

The video algorithms require a parallel implementation so the MicroBlaze processor was not selected for implementing this part of the design. The algorithms required to translate the video signals could be written using VHDL and would meet the speed required, but that would take a considerable amount of time- a faster method needed to be found to 'pound out' these high level video algorithms. The Celoxica FPGA design tools allow the designer to write the code for the algorithm in C and compile it directly to FPGA gates. This results in a parallel hardware implementation, hits the performance required and only takes days to develop, not the weeks a VHDL implementation would require.

Celoxica™ DK1 Design Suite Description

Software engineers and system architects can significantly reduce design cycle time and increase performance of FPGA-based system designs by using the Celoxica DK1 design suite - a direct C-to-hardware design methodology. DK1 features Handel-C, an ANSI-C-based language with simple extensions for hardware design. DK1 represents a significant breakthrough in FPGA-based system designs. It enables system architects, software engineers, and hardware engineers with C knowledge to dramatically improve design team productivity and meet demanding time-to-market requirements. (Avnet Design Services sells the Celoxica DK1 Design Suite to accelerate the time to market for FPGA designs with algorithmic processing requirements. For more information visit www.ads.avnet.com and click on Avnet Ave.)

Video Processing Peripheral via ADS Virtex™-E Development Kit

The video processing peripheral is show in Figure 2. An Avnet Design Services Virtex-E Development Kit is used to host the application in a prototype form. The Virtex-E Development Kit provides a complete hardware development environment for FPGA or system designers to accelerate their time to market. With the extensive hardware functions available on the kit, you can begin your FPGA design or applications code development right away, with no need to wait for prototype circuit boards. Unlike other boards that only offer only one or two I/O ports, no memory and little expansion capability, the Virtex-E Development Kit offers a majority of functions usually required, as well as the ability to add custom hardware via the PCI bus, a PC card connector, PCI mezzanine connector, and the AvBus™ modular hardware expansion connectors. This kit provides it all, with extensive on board functionality and unmatched expansion capability.

Avnet Design Services has assembled an extensive group of industry leading integrated circuits suppliers, applications code developers, and web partners, as well as IP Cores, device drivers, development tools, and test equipment, to support the Virtex-E Development Kit. Our partners have chosen the Virtex-E Development Kit as their system development environment of choice. Visit www.ads.avnet.com for a current list of our partners, along with their support products and services available to help speed your development cycle.

Virtex-E Development Kit Features

The Virtex-E Development Kit incorporates a variety of hardware resources on a single PCI form factor printed circuit board to create a powerful FPGA and system design development environment. Included on the board are the following hardware resources:

- FPGA / Interfaces
  - Xilinx® Virtex™-E XCV1000E-6FG1156 (660 I/O) (expandable up to the XCV3200E, 804 I/O)
  - Controlled impedance board and I/O connectors
  - 64-Bit/33Mhz, PCI Bus standard interface connector (+3.3 VDC)
  - Supports PCI mezzanine cards (IEEE Std. 1386) (+3.3VDC)
  - AvBus™ daughtercard connectors (5 -140 pin AMP #179031-6)
  - PC card connector
- Memory
  - 64 MByte Micron® SDRAM (Four 16MByte x 16-Bit x 4 banks, to form a 64-Bit bus)
  - 32 MByte Flash (Four 8MByte x 16-Bit, to form a 64-Bit bus); sites for both AMD and Intel +5.0 VDC and +3.3 VDC) components
  - Bi-directional RS-232 interface (UART core internal to FPGA)
  - CAN bus interface (CAN core internal to FPGA)
  - 10/100 PHY interface (w/MAC core internal to FPGA)
  - Optional USB 2.0 (and 1.1 compliant) transceiver with one upstream and one downstream connector (USB core internal to FPGA)
- Video / Audio
  - PAL/NTSC/SECAM Video Decoder
  - 80MHz, 256X24 Color Palette, Triple, 6-bit Video Converter, RAM-DAC
  - 192Khz 24 Bit Stereo DAC

- Miscellaneous
  - 8 DIP switches
  - 3 push-buttons
  - 8 LEDs
- Power
  - On-card power regulation derived from +9.0 VDC
  - +5.0 VDC used to create +3.3 VDC and +1.8 VDC
  - PCI +5.0 VDC option to power card
  - PC card power management controller
- Programming Options
  - Xilinx Serial / Parallel download port
  - FLASH based parallel FPGA loading (SelectMAP)
  - JTAG port

Conclusion

The entire Video Processing Peripheral can be implemented using several of the time to market oriented kits, IP Cores and design software available from Avnet Design Services. The ability to select from this large set of application modules makes it easy to develop prototype hardware in record time. Applications code, and firmware can be quickly developed on top of the hardware platform while investigating architectural alternatives. No other development environment offers such speed and flexibility.

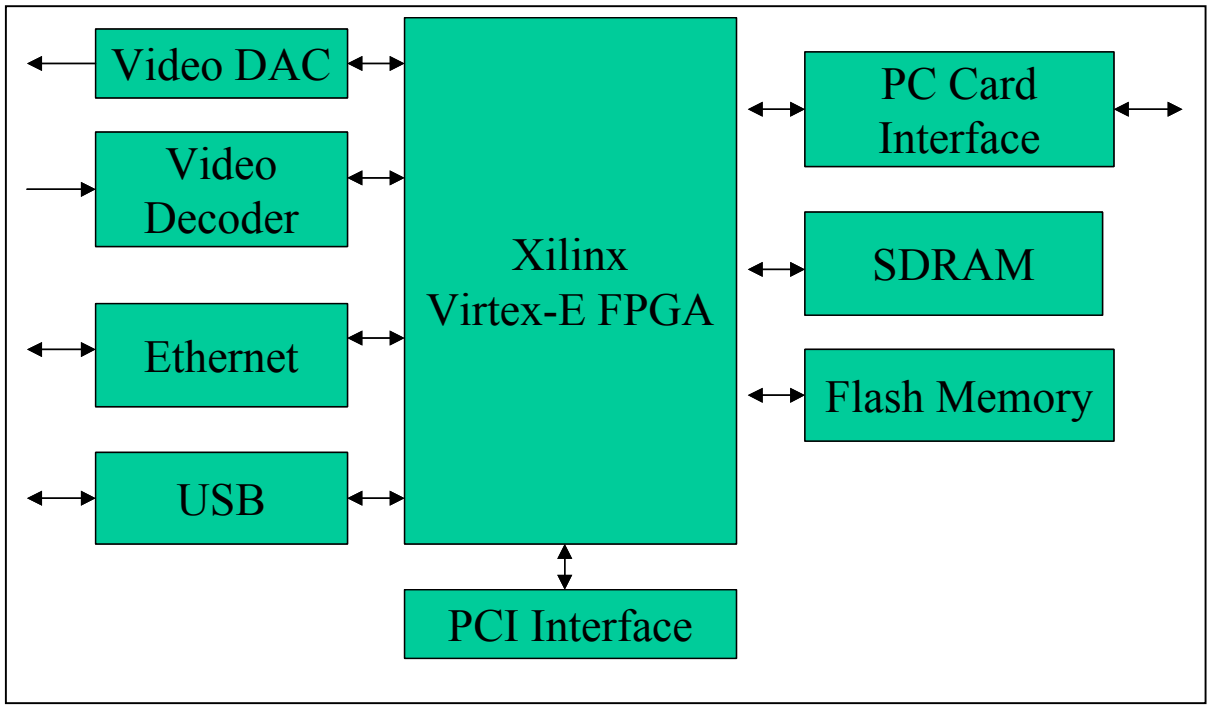

Figure 1: System Level Block Diagram

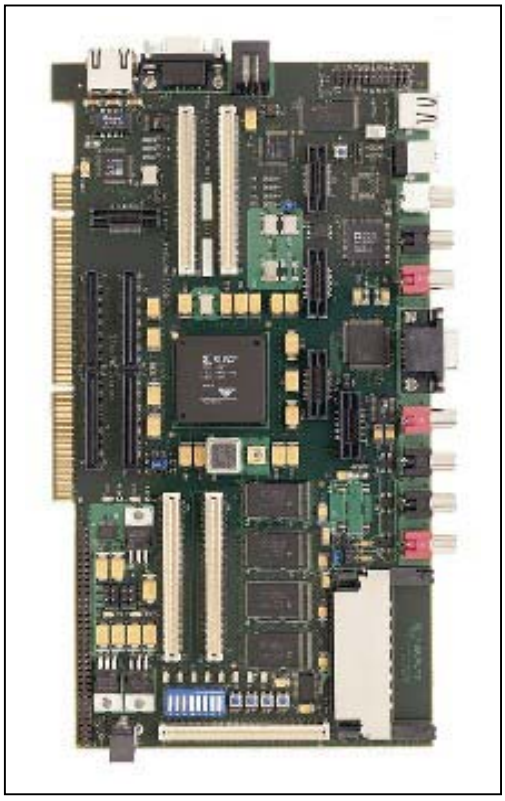

Figure 2: Video Processing Peripheral Prototype using Avnet Design Services Development Board